

FIG. 1 (Prior Art)

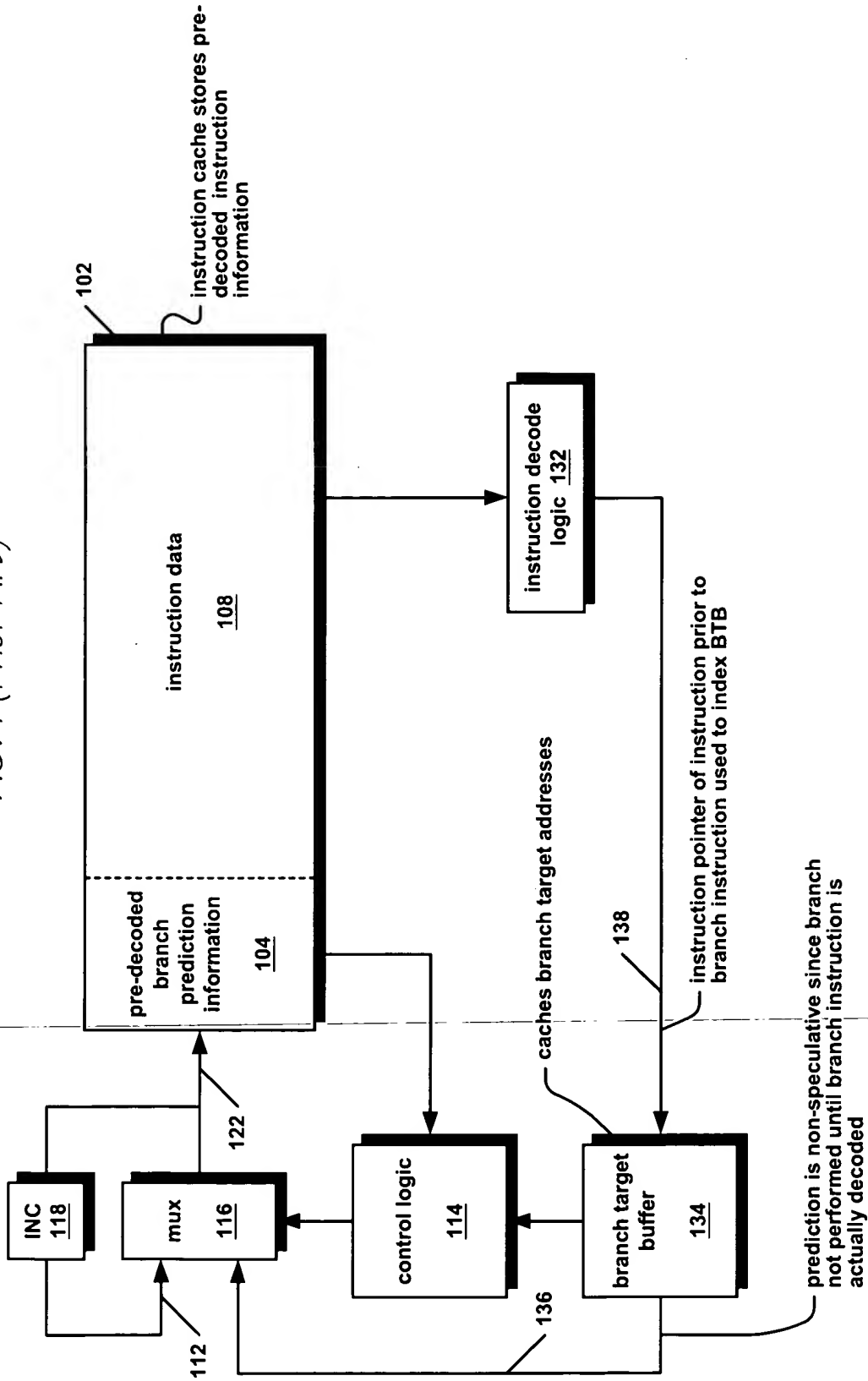
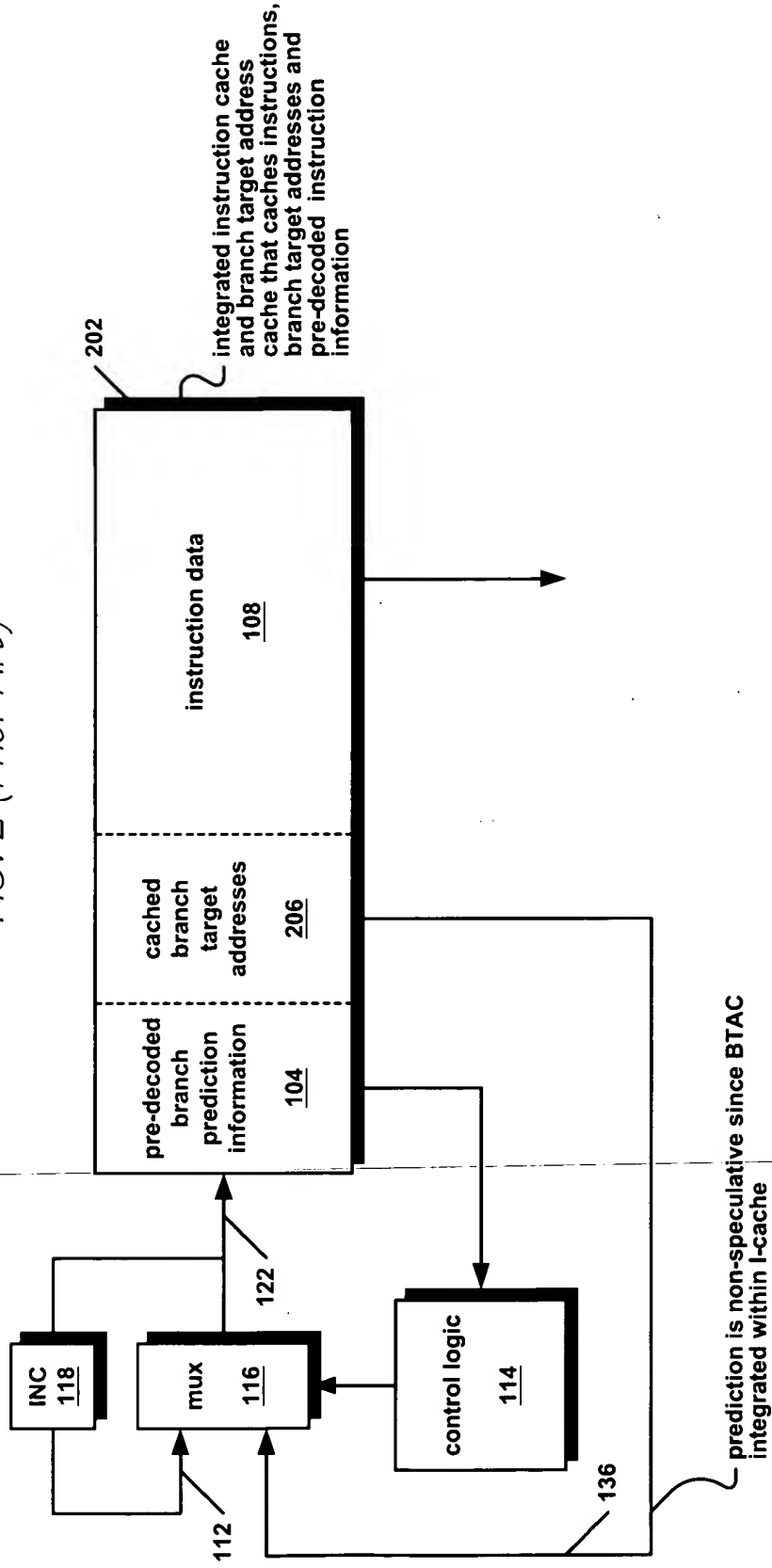
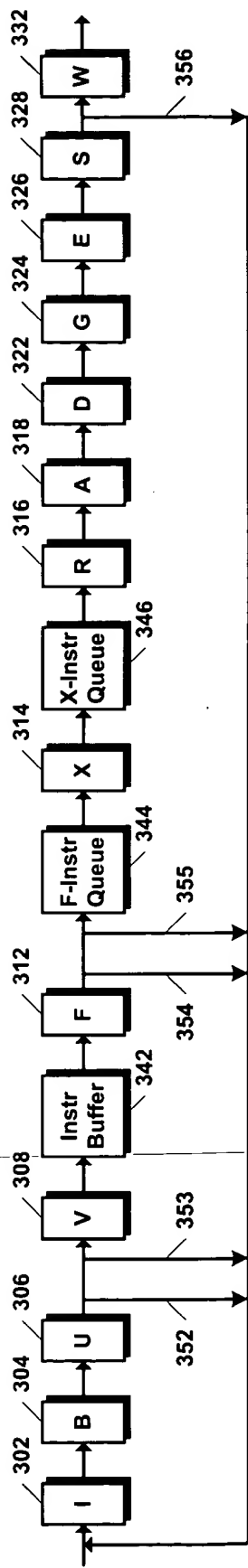


FIG. 2 (Prior Art)



Athlon BTAC Integrated into Instruction Cache

FIG. 3



300

Processor Pipeline Stages

FIG. 4

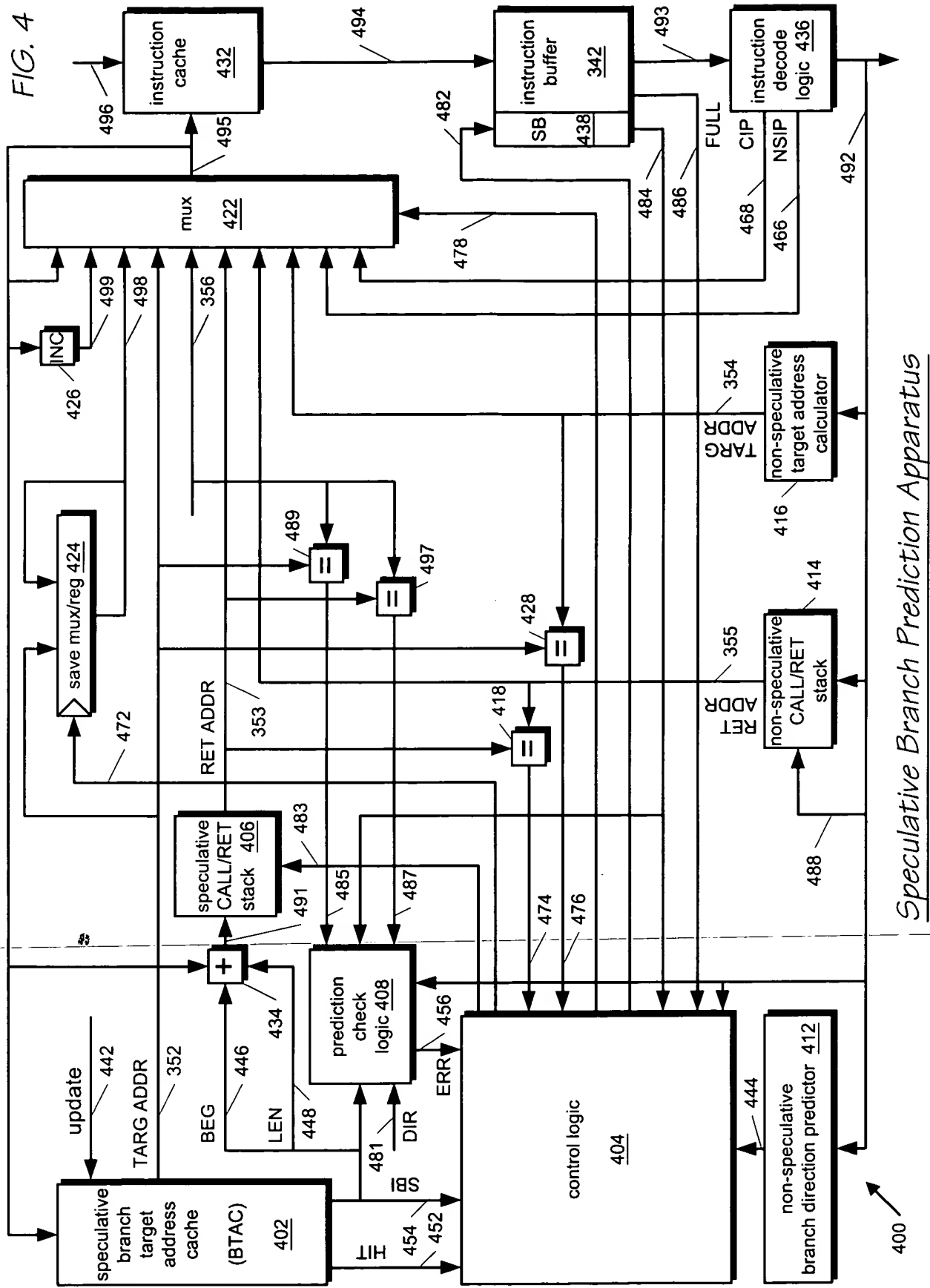
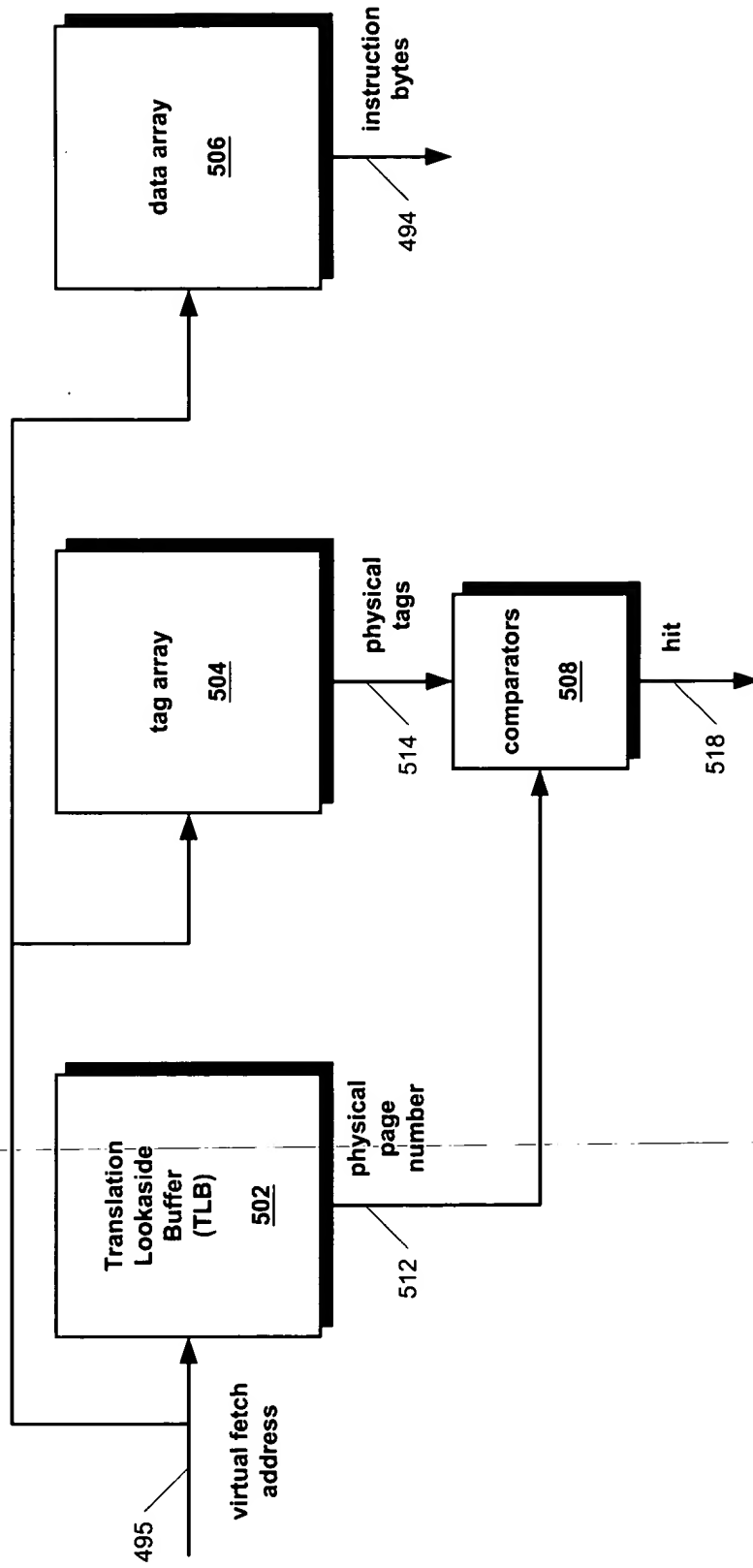
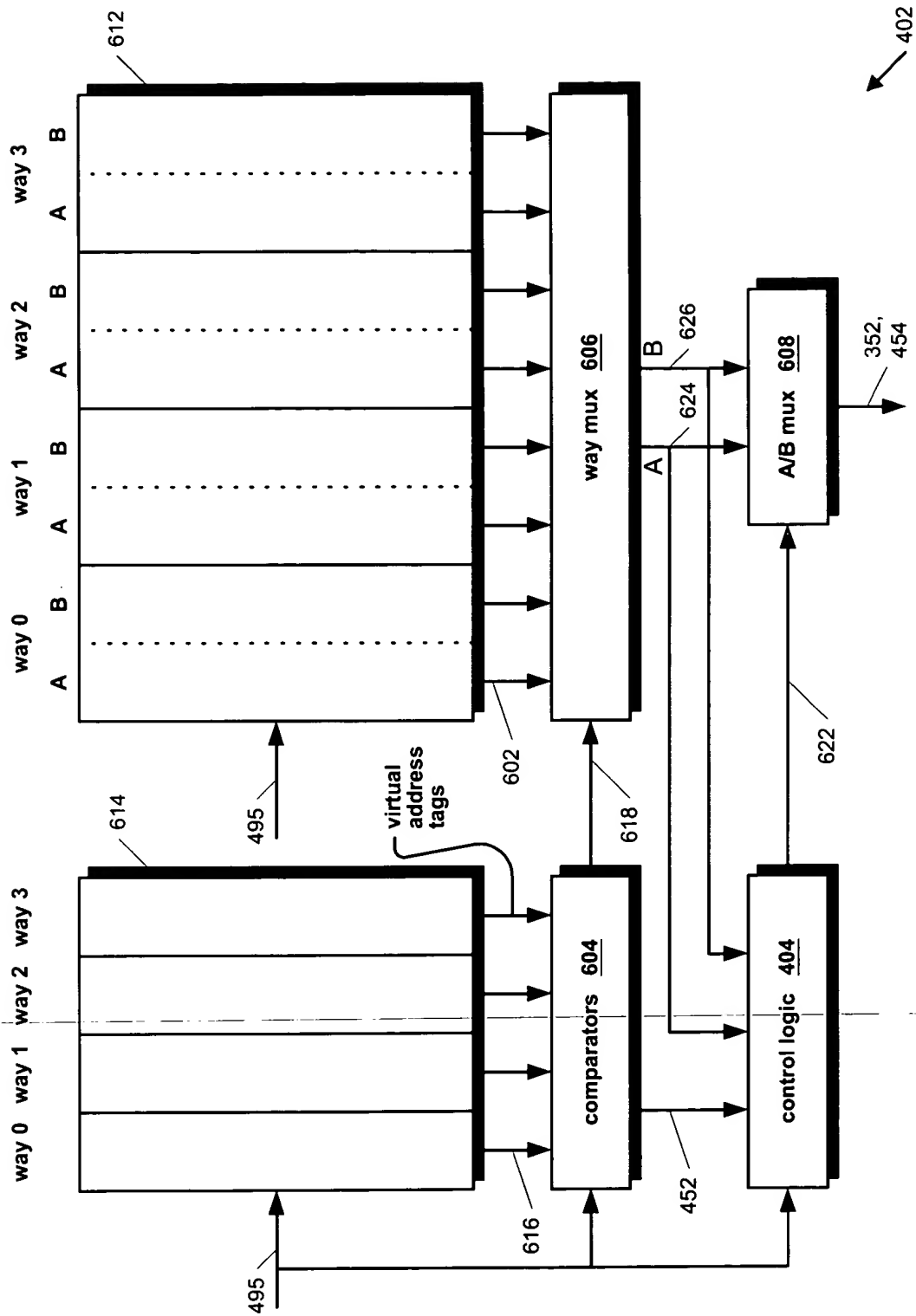


FIG. 5



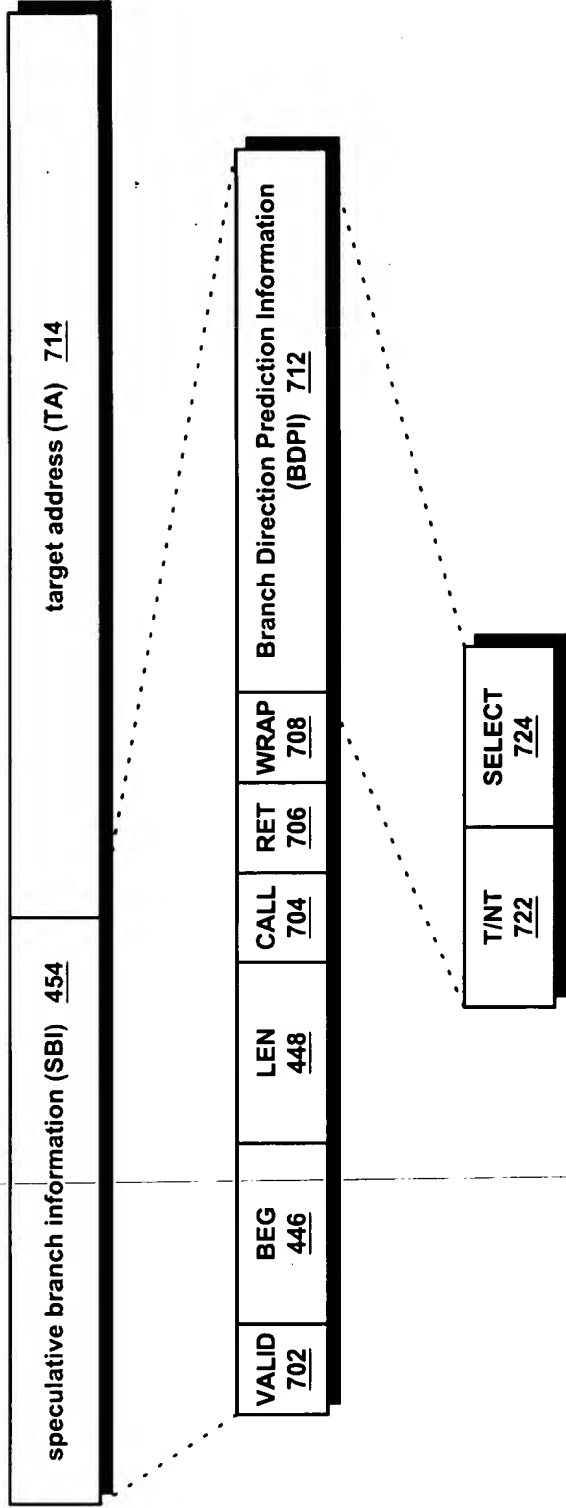
Instruction Cache

FIG. 6



BTAC

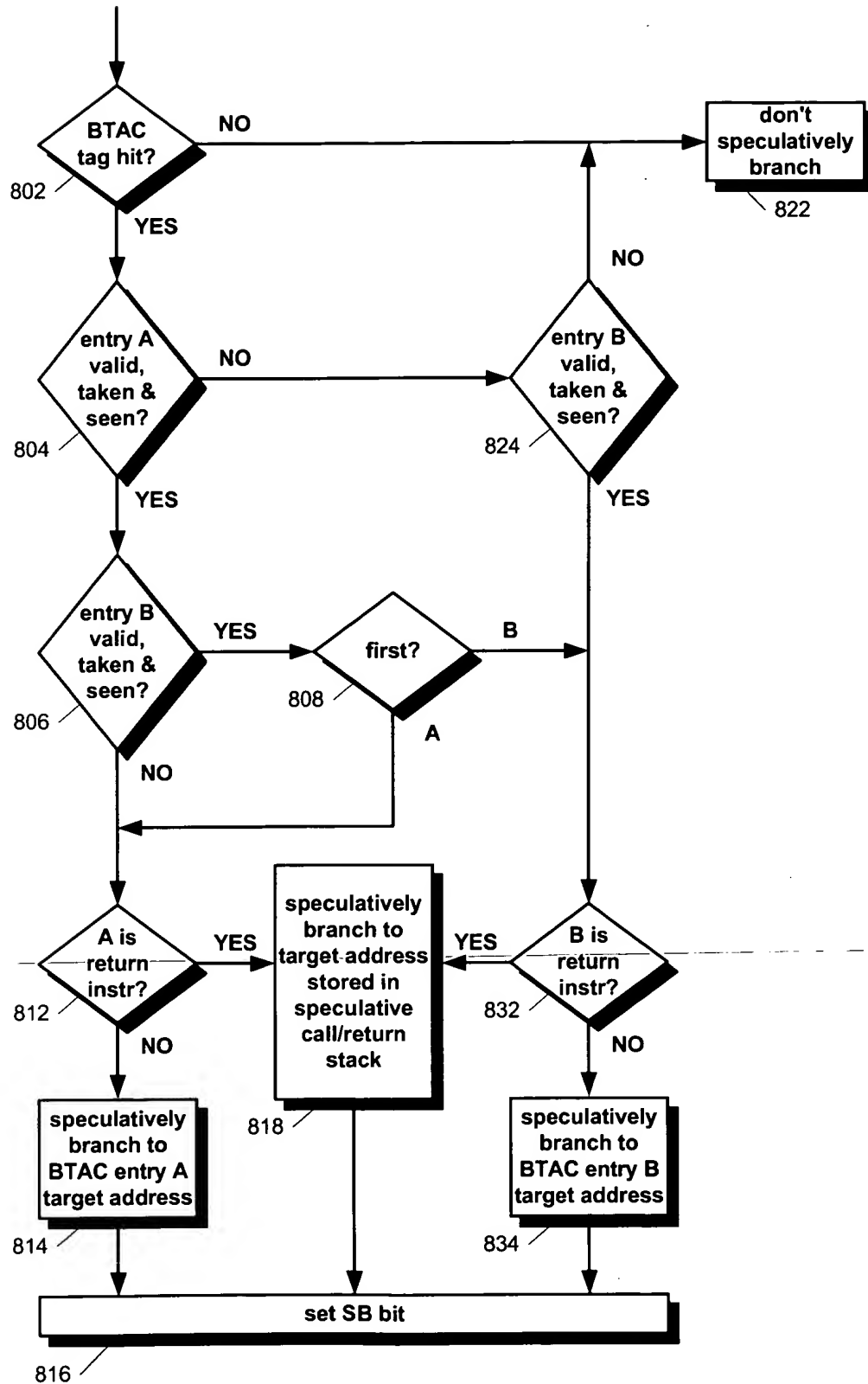
FIG. 7



602

BTAC Entry

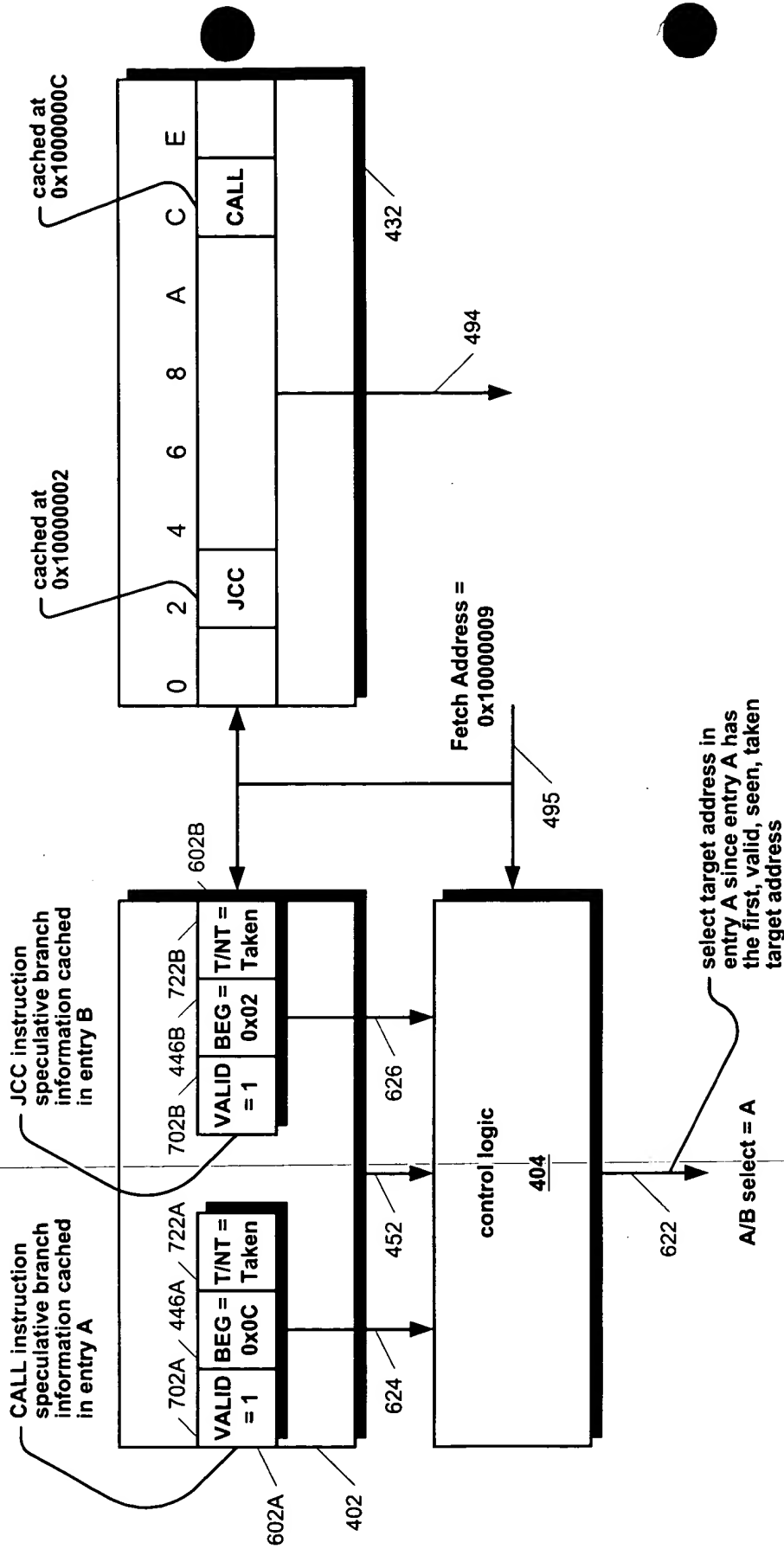
FIG. 8



Speculative Branching Operation

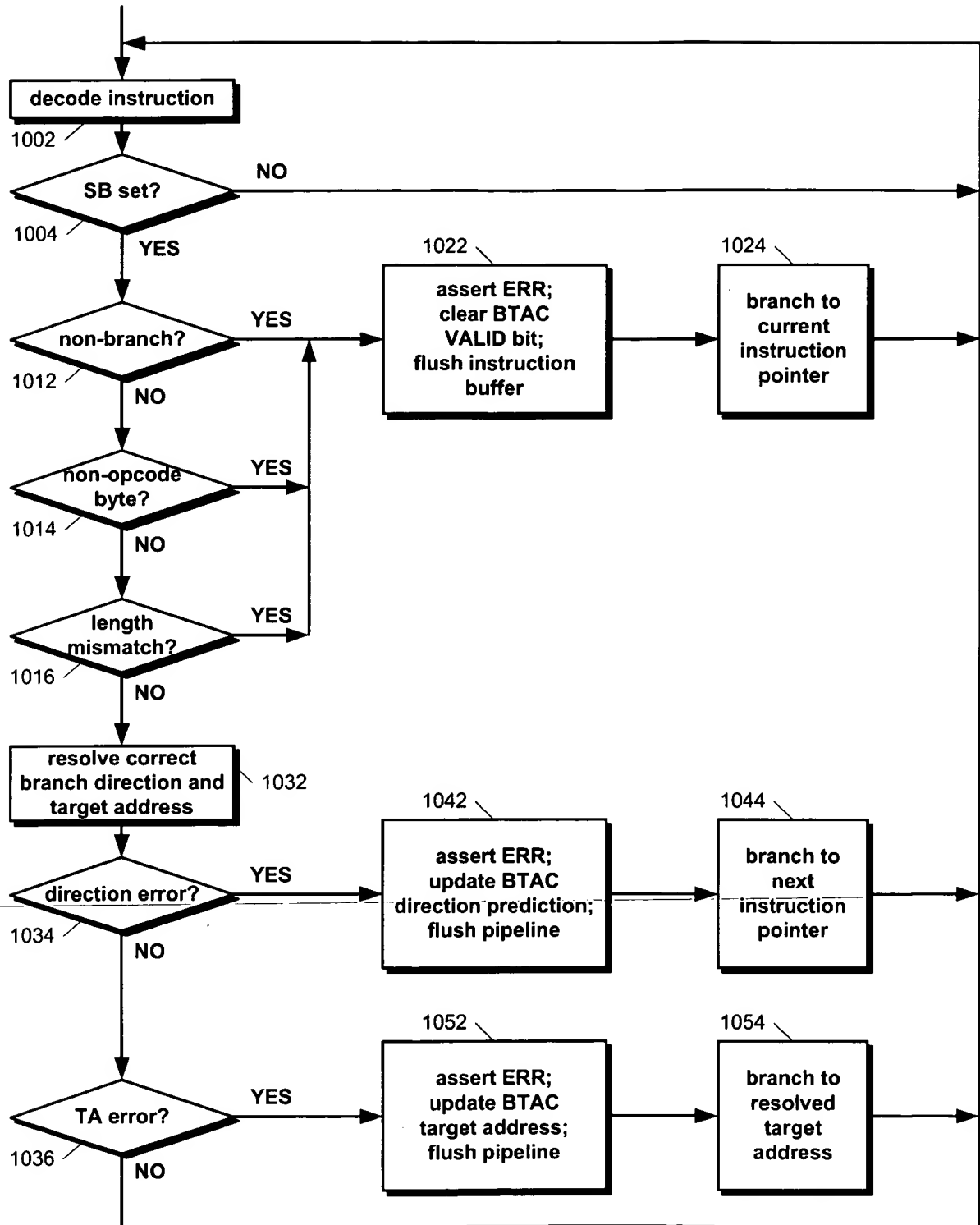


FIG. 9



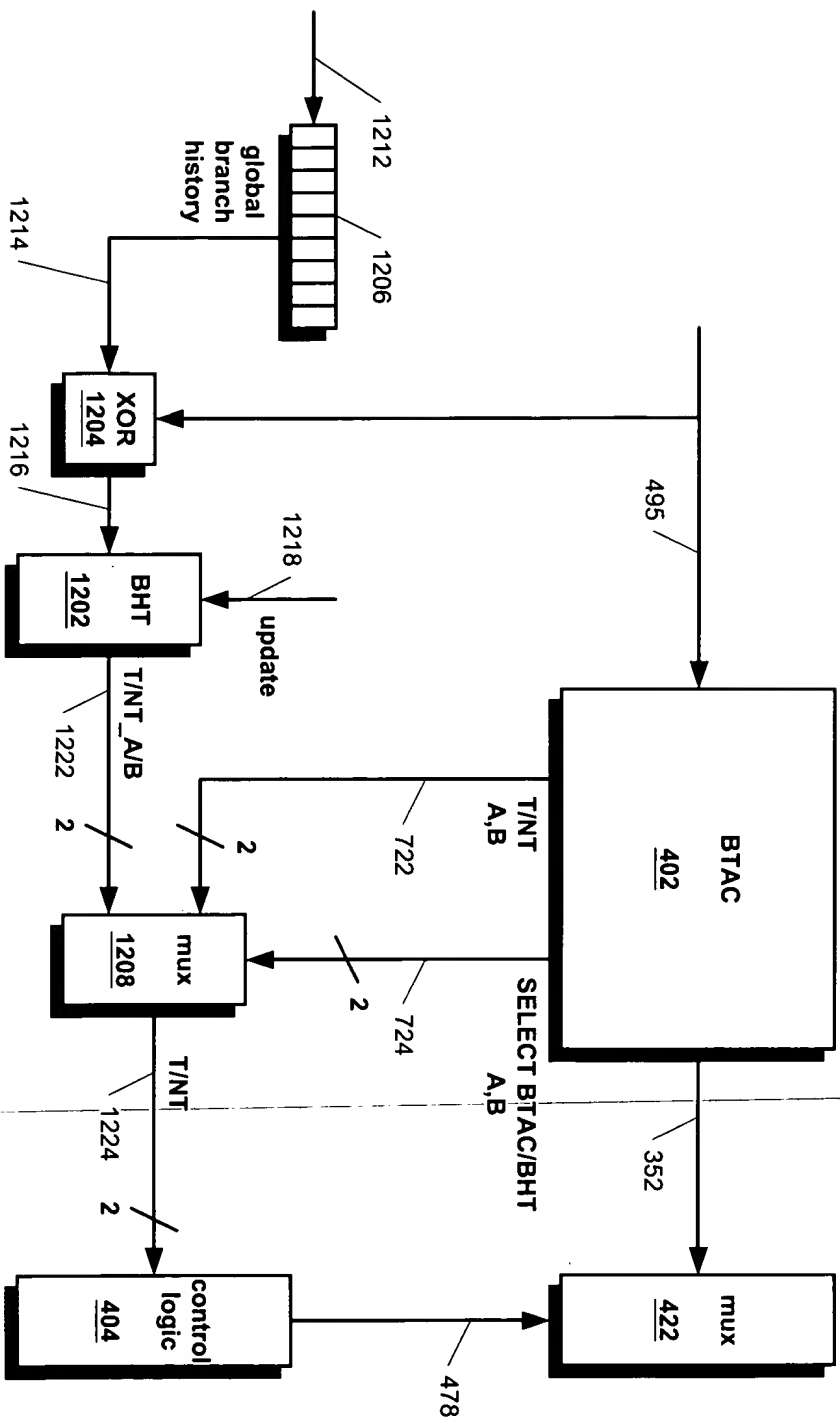
Target Address Selection Example

FIG. 10



Detection and Correction of  
Speculative Branch Misprediction

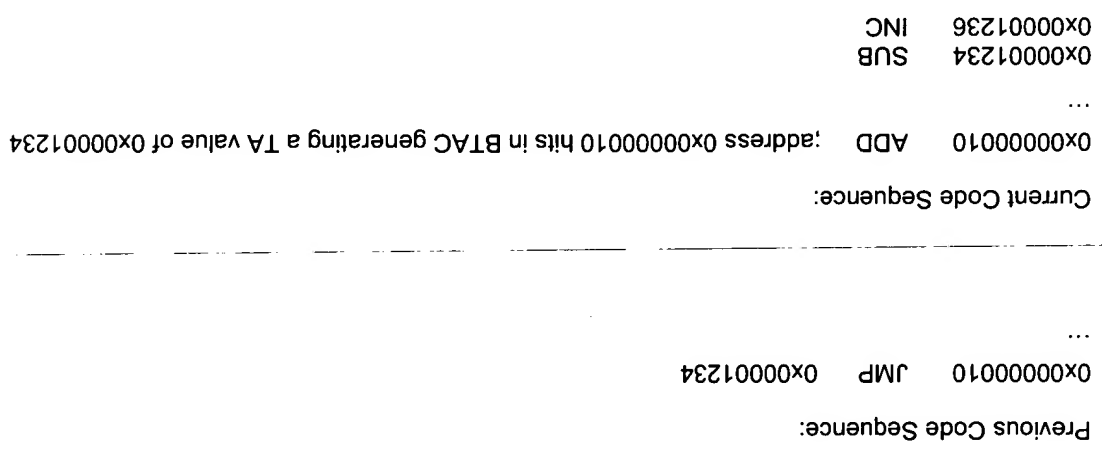
FIG. 12



1200

Hybrid Speculative Branch Direction Predictor

FIG. 11

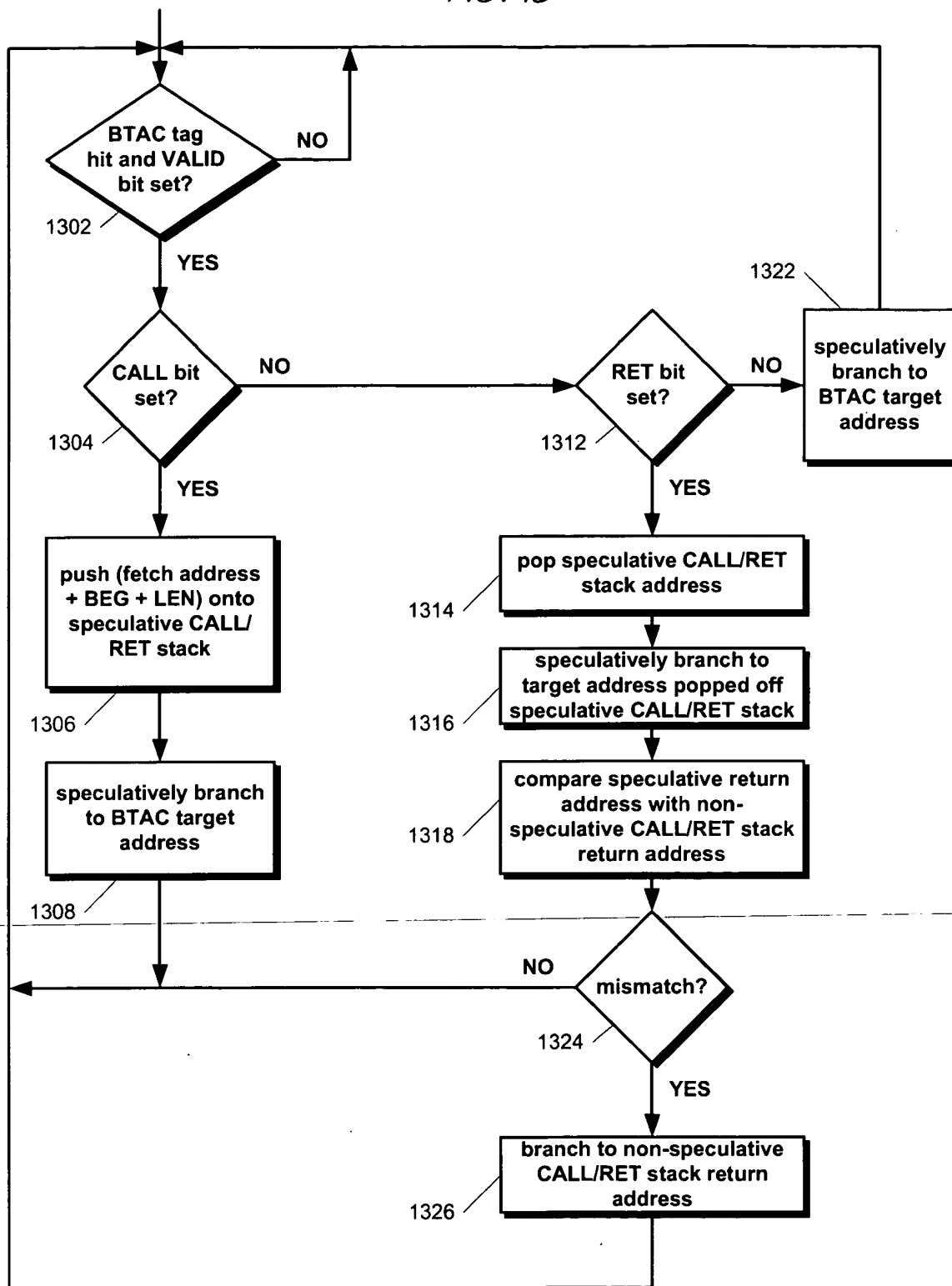


|         |     |     |     |     |     |   |     |
|---------|-----|-----|-----|-----|-----|---|-----|
| clock → | 1   | 2   | 3   | 4   | 5   | 6 | 7   |
| I-stage | ADD | X   | X   | SUB | INC | X | ADD |
| B-stage |     | ADD | X   | X   | SUB | X | X   |
| U-stage |     |     | ADD | X   | X   | X | X   |
| V-stage |     |     |     | ADD | X   | X | X   |
| F-stage |     |     |     |     | ADD | X | X   |

Cycle 1 = BTAC and I-cache access cycle  
Cycle 4 = speculative branch cycle  
Cycle 5 = speculative branch error detection cycle  
Cycle 6 = BTAC invalidate cycle  
Cycle 7 = speculative branch error correction cycle

1100 ↘

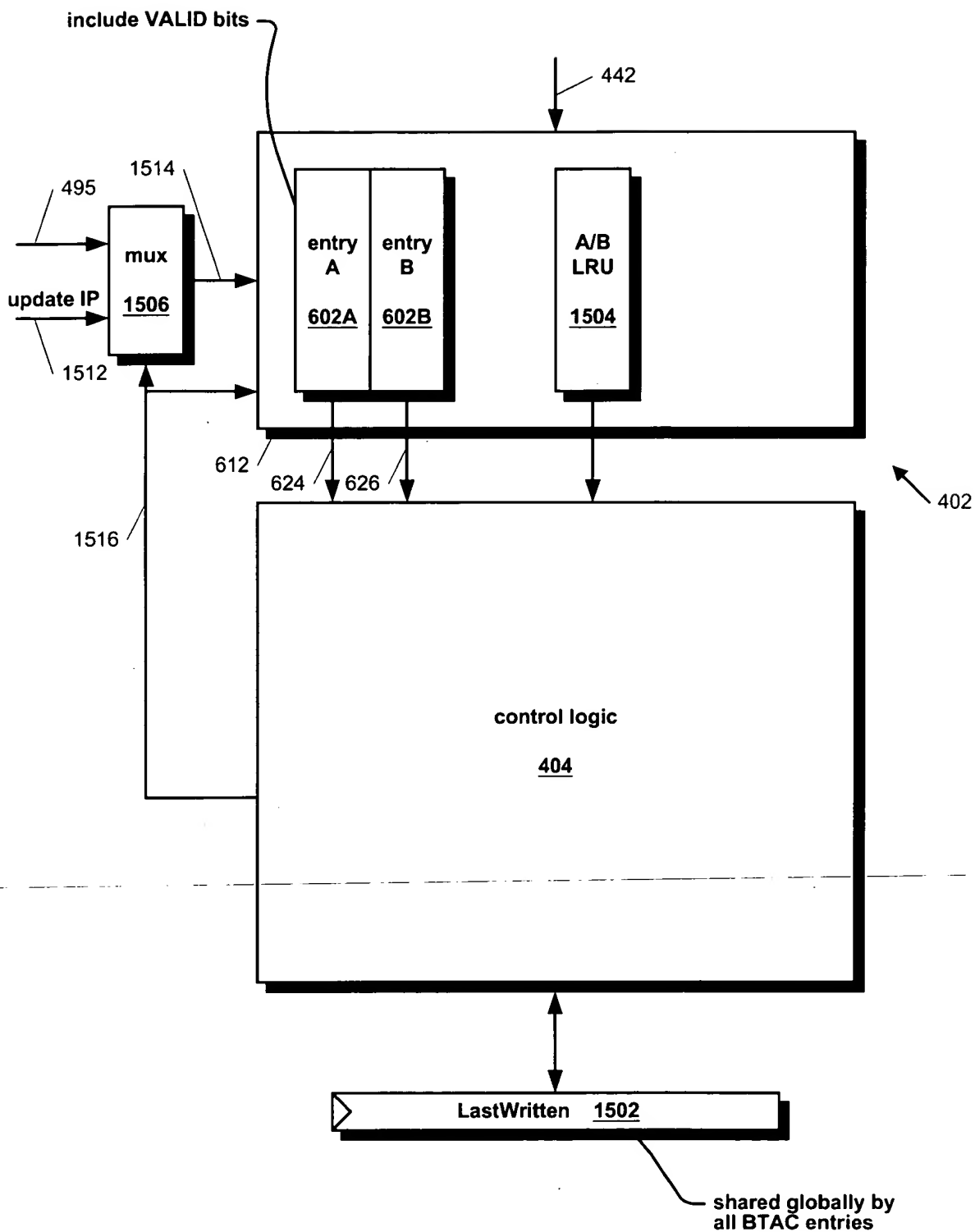
FIG. 13



Dual CALL/RET Stack Operation

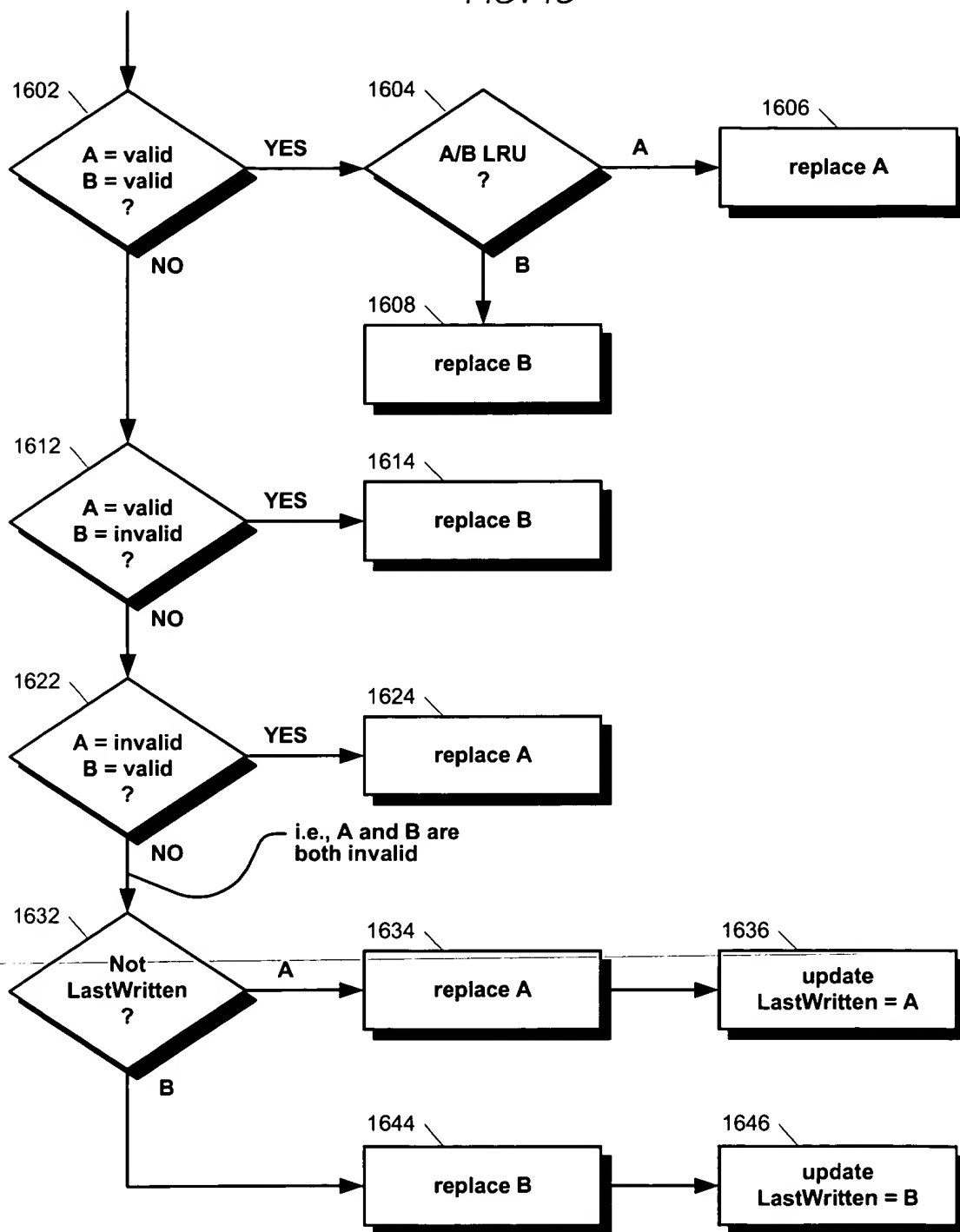
[illegible]

FIG. 15



BTAC A/B Replacement Apparatus

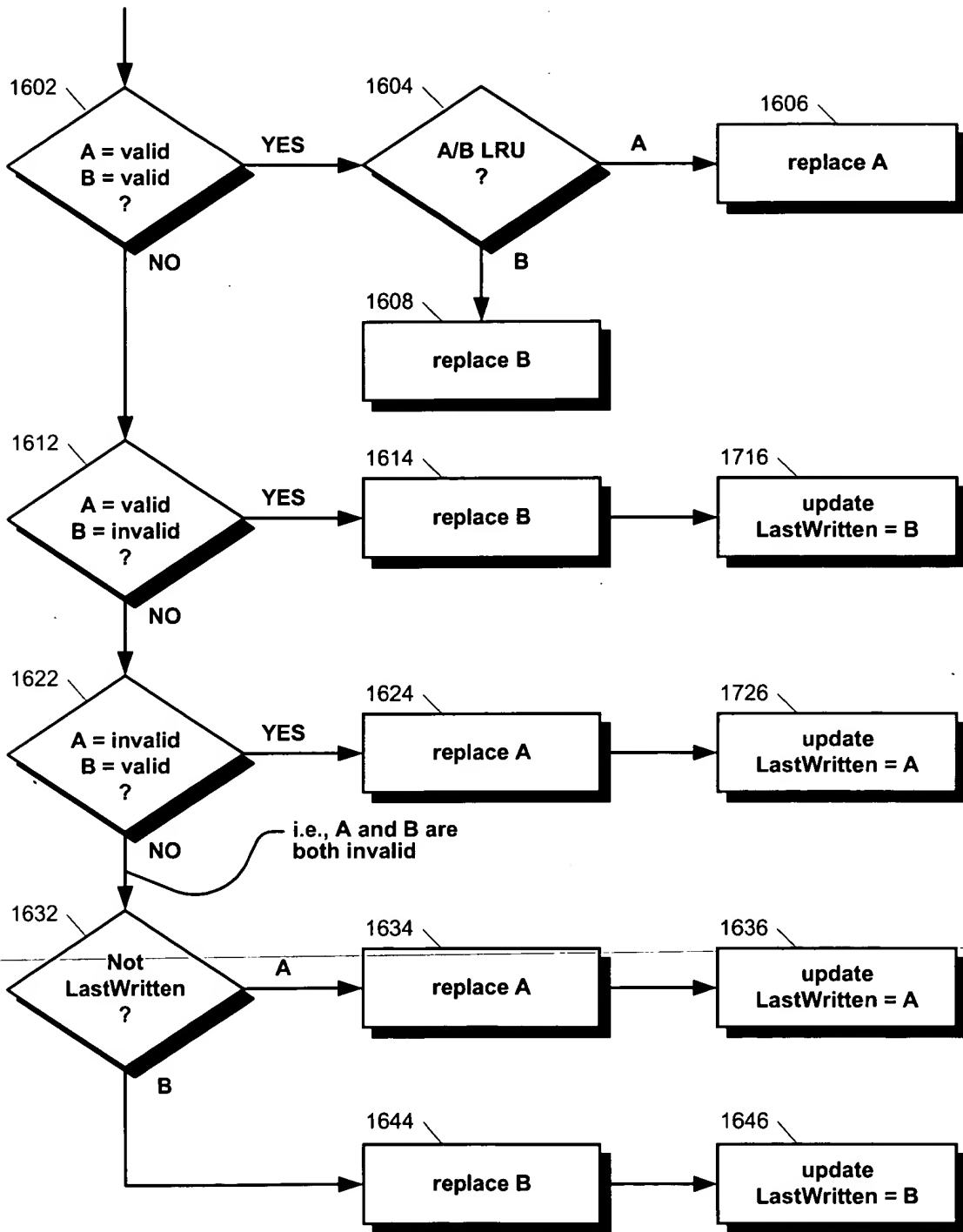
FIG. 16



A/B Entry Replacement Method

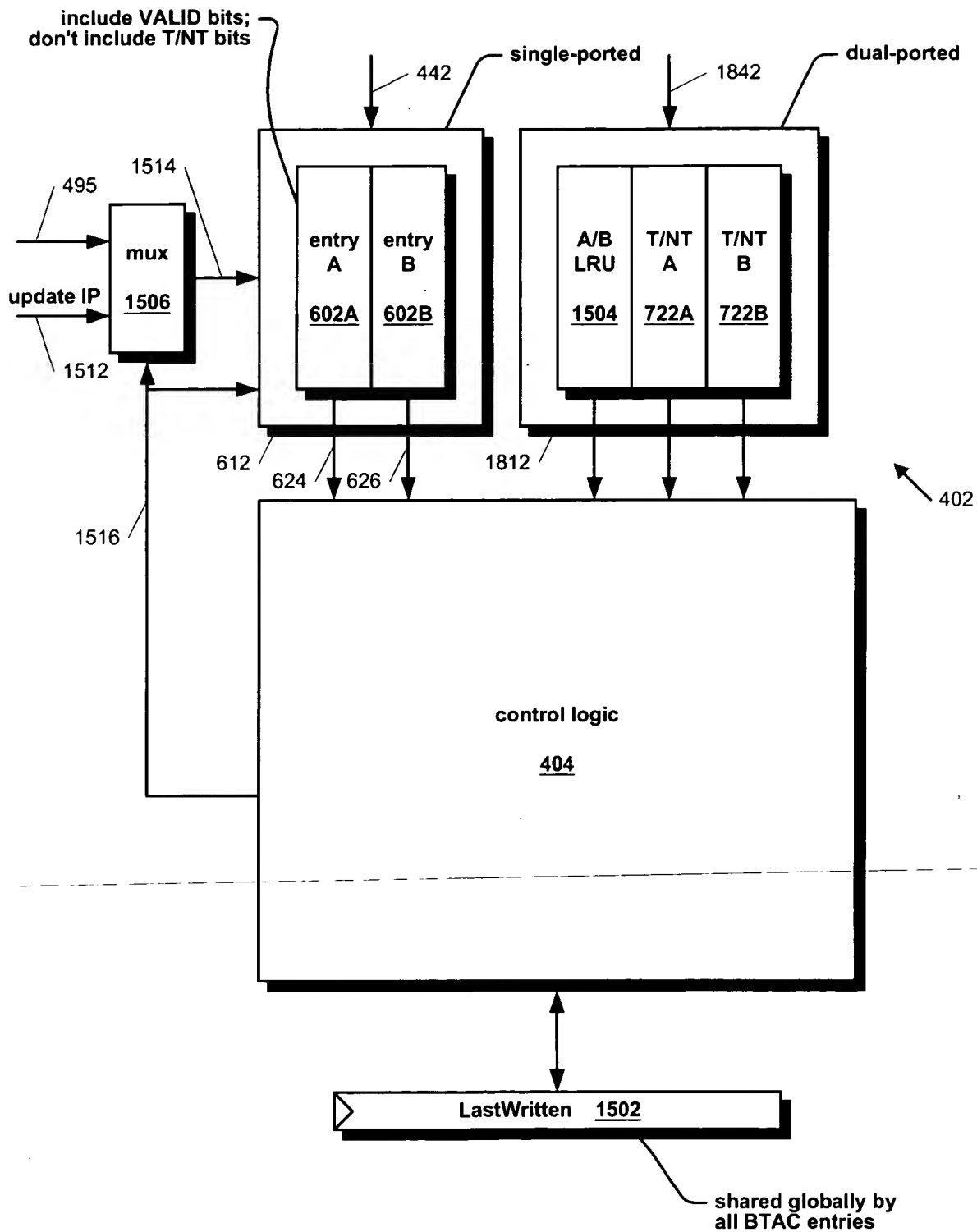


FIG. 17



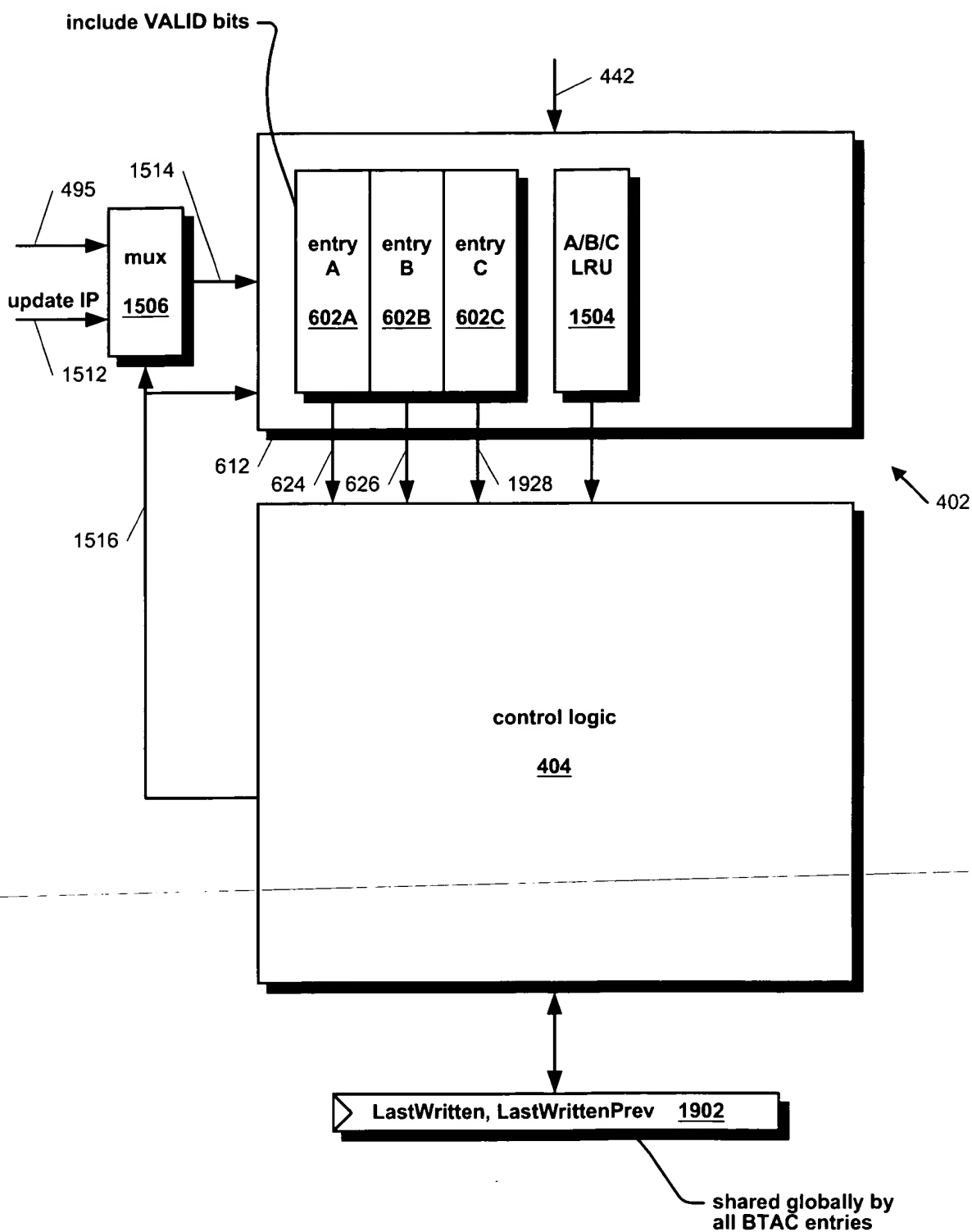
A/B Entry Replacement Method (Alt. Embodiment)

FIG. 18



BTAC A/B Replacement Apparatus (Alt. Embodiment)

FIG. 19



BTAC A/B/C Replacement Apparatus